WHAT IS CLAIMED IS:

1. A system for recovering timing information from a serial data signal, comprising:

a phase interpolator adapted to derive a sampling signal having an interpolated phase in response to a plurality of control signals; and

a controller including

a data path adapted to sample the serial data signal according to the sampling signal,

a phase detector adapted to detect a phase offset between the sampling signal and the serial data signal,

a phase error processor coupled to the phase detector and adapted to estimate a frequency offset between the sampling signal and the serial data signal based on the phase offset,

a command generator coupled to the phase error processor and adapted to generate a rotator control signal in response to the frequency offset estimate, and

a control signal rotator adapted to manipulate the control signals in response to the rotator control signal, whereby the controller causes the phase interpolator to rotate the interpolated phase of the sampling signal at a rate corresponding to the frequency offset.

2. A system for recovering timing information from a serial data signal, comprising:

a phase interpolator adapted to derive a sampling signal having an interpolated phase; and

a controller coupled to the phase interpolator and including

a phase error processor adapted to derive an estimate of a frequency offset between the sampling signal and the serial data signal, the controller being adapted to cause the phase interpolator to rotate the interpolated

phase of the sampling signal at a rate corresponding to the frequency offset so as to reduce the frequency offset between the sampling signal and the serial data signal.

3. The system of claim 2, wherein the controller causes the phase interpolator to repetitively rotate the interpolated phase of the sampling signal through a range of phases spanning 360° at the rate corresponding to the frequency offset.

4. The system of claim 2, wherein the controller includes logic adapted to cause the phase interpolator to:

rotate the interpolated phase of the sampling signal in a direction of increasing phase to decrease a frequency of the sampling signal when the frequency offset estimate indicates a frequency of the sampling signal is greater than a frequency of the serial data signal; and

rotate the interpolated phase of the sampling signal in a direction of decreasing phase to increase the frequency of the sampling signal when the frequency offset estimate indicates the frequency of the sampling signal is less than a frequency of the serial data signal.

5. The system of claim 2, wherein the phase interpolator includes:

a plurality of reference stages adapted to control individual magnitudes of a plurality of component signals having different phases responsive to a plurality of control signals; and

a combining node adapted to combine the plurality of component signals into the interpolated timing signal.

6. The system of claim 2, wherein the controller includes:

a data path adapted to sample the serial data signal according to the sampling signal, thereby producing serial data samples;

a phase detector coupled to the phase error processor and adapted to detect a phase offset between the sampling signal and the serial data signal based on the serial data signal, the phase error processor being adapted to estimate the frequency offset between the sampling signal and the serial data signal based on the phase offset.

7. The system of claim 2, wherein the controller includes a phase detector adapted to detect a phase offset between the sampling signal and the serial data signal, the phase error processor being adapted to estimate the frequency offset between the sampling signal and the serial data signal based on the phase offset.

8. The system of claim 2, wherein the controller is adapted to apply a plurality of phase control signals to the phase interpolator to control the interpolated phase of the sampling signal, the controller being adapted to manipulate the plurality of phase control signals, and correspondingly, the interpolated phase of the sampling signal, based on the frequency offset estimate.

9. The system of claim 8, wherein the controller is adapted to rotate the plurality of phase control signals, and correspondingly, the interpolated phase of the sampling signal according to the frequency offset estimate.

10. The system of claim 2, wherein the controller further includes:

a command generator coupled to the phase error processor and adapted to generate a rotator control signal in response to the frequency offset estimate; and

a control signal rotator adapted to apply a plurality of phase control signals to the phase interpolator to control the interpolated phase of the sampling signal, the control signal rotator being adapted to rotate the plurality of phase control signals, and correspondingly the interpolated phase of the sampling

signal, at the rate corresponding to the frequency offset, responsive to the rotator control signal.

11. The system of claim 10, wherein the rotator control signal is one of a phase-advance, a phase-retard, and a phase-hold signal, the phase control signal rotator being adapted to:

rotate the plurality of controls signals in a first direction to advance the interpolated phase of the timing signal in response to the phase-advance signal;

rotate the plurality of controls signals in a second direction to retard the interpolated phase in response to the phase-retard signal; and

prevent the plurality of phase control signals and correspondingly the interpolated phase from rotating in response to the phase-hold signal.

12. A method of recovering timing information from a serial data signal, comprising:

(a) deriving a sampling signal having an interpolated phase;

(b) estimating a frequency offset between the sampling signal and the serial data signal; and

(c) rotating the interpolated phase of the sampling signal at a rate corresponding to the frequency offset, thereby reducing the frequency offset between the sampling signal and the serial data signal.

13. The method of claim 12, wherein step (b) comprises:

detecting a phase offset between the serial data signal and the sampling signal; and

estimating the frequency offset based on the phase offset.

14. The method of claim 12, wherein step (c) comprises repetitively rotating the interpolated phase of the sampling signal through a range of phases spanning 360° at the rate corresponding to the frequency offset.

15. The method of claim 14, wherein step (c) further comprises:

rotating the interpolated phase of the sampling signal in a direction of increasing phase to decrease a frequency of the sampling signal when the frequency of the sampling signal is greater than a frequency of the serial data signal; and

rotating the interpolated phase of the sampling signal in a direction of decreasing phase to increase the frequency of the sampling signal when the frequency of the sampling signal is less than the frequency of the serial data signal.

16. The method of claim 12, wherein step (a) comprises deriving the sampling signal phase responsive to a plurality of phase control signals, the method further comprising manipulating the plurality of phase control signals responsive to the phase offset.

17. The method of claim 16, wherein:

step (a) comprises deriving the sampling signal phase responsive to a plurality of phase control signals; and

step (c) comprises rotating the plurality of phase control signals, and correspondingly, the interpolated phase of the sampling signal according to the phase offset.

18. The method of claim 12, wherein step (b) comprises:

sampling the serial data signal according to the sampling signal, thereby producing serial data signal samples;

deriving a frequency error signal indicative of the frequency offset between the timing signal and the serial data signal based on the serial data signal samples.

19. The method of claim 12, wherein step (a) comprises:

controlling individual magnitudes of a plurality of component signals having different phases responsive to a plurality of phase control signals; and

combining the plurality of component signals into the sampling signal having the interpolated phase.

20. The method of claim 12, wherein step (c) comprises synchronizing a frequency of the sampling signal to a frequency of the serial data signal.